Classification showcase ICD

Motto: Fundamental Solutions for Practical Problems
A random selection of realized setups in mainly CMOS technology.

Receiver:

Noise reduction:
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- Analog: Wide Band Low-Noise Amplifier Techniques in CMOS: Federico Bruccoleri Chip?
- Digital: RF Spectrum Sensing in CMOS exploiting cross correlation: Mark Oude Alink Chip?
- Physically: LF noise under large signal excitation: Arnoud van der Wel

Datatransmission:

- On-Chip communication: Eisse Mensink UTnanochip2
- On-Chip Data communication: Daniël Schinkel UTnanochip 1 en 2
- On PCB: Wireline Equalization using Pulse-Width Modulation: Jan Rutger Schrader

AD converter and (sub)sampling:

- Low power A/D conversion: Michiel van de Elzakker
- Low jitter subsampling: Gao
- Low Energy Design Techniques: Harijot Singh Bindra (chipfoto vragen) filmpje!
- High Speed Low Jitter Frequency Multiplication: Remco van de Beek
-

N-Path Filters:

- Active N-Path filters: Milad Darvishi,
- Switched RC-Radio Frequency N-path Filters: Amir Ghaffari

Circuit/System receiver Solutions:

- IoT Receiver Techniques: Bart Thijssen
- Switched RC Beamforming Receiver in Advanced CMOS: Michiel Soer
- Interference Mitigation for MIMO Receivers: Sayad Golabi
- Wide Band Linearization Techniques for RF Receiver Front-Ends: Anoop Bhat
- DtC for spur correction in Digital Frequency Synthesis: Claudia Palattella
- Analog front-ends for software defined radio receiver: Vincent Arkesteijn

Transmitter:

RF

- Switched Mode Class E Power Amplifiers: Ali Ghahremani
- Self-Matching Balanced Amplifier: Anton Atanasov
- Voltage Boosting Amplifier Techniques: Saifullah Amir

Audio:

- Active PWM Ripple Reduction in Class-D Amplifiers: Chris Lokin
-

Optisch elektronisch:

- High speed photodiodes in standard CMOS: Sasa Radovanovic
- Optics in: Vishal Agarwal
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RECEIVERS

1: Spatial and frequency domain filtering.

Dirk-Jan van de Broek:

CMOS Front-End Techniques for In-Band Full-Duplex Radio @ 2017

Demonstrating techniques usin£g vector modulator downmixers to cancel Self Interference in full duplex front-ends.

Technology: 22nm FD-SOI

Sayad:

Interference mitigation MiMO receivers @2022

Application of analog digital beamforming before ADC's can mitigate interference

Technology: 22nm FD-SOI

2: N-path filters:

Amir Ghaffari:

Switched-RC Radio Frequency N-Path Filtering @2013

Technology: 65nm CMOS

Michiel Soer:

Switched-RC Beamforming Receivers in Advanced CMOS @2012

Technology: 65nm CMOS

Milad Darvishi:

Design of 6 Path BandPass Filter rejecting the 2nd and 3rd harmonic @2012

Applying N-path Filters to realize high-Q Bandpass Filters with a wide tunabilty of the centerfrequency, it depends on the clock frequency.

Technology: 65nm CMOS

3: Noise reduction:

Federico Bruccoleri:

Wide Band Techniques in CMOS @2003

Wide band Low Noise Amplifier with noise cancelling.

Technology: 0.35µm CMOS

Arnoud van de Wel:

MOSFET LF noise under large signal excitation @2005

Study on Large excitation signal at MOSFETs to reduce LF Noise (1/f).

Technology: large (µm2) to much smaller CMOS transistors

Mark Oude Alink:

RF Spectrum Sensing in CMOS Exploiting Cross correlation @2013

Carrying out RF spectrum analysis on CMOS-chip and apply cross correlation to increase SNR or by lowering the reduce power consumption at low SNR.

Technology: 65nm CMOS

4: AD converter and (sub)sampling:

Michiel van de Elzakker:

New comparator architecture based on charge redistribution.
4.7 fJ/conversion-step a world record in @2013
Technology: 65nm CMOS

Harijot Singh Bindra:

Low Energy Design Techniques for Data Converters @2019
Design techniques to reduce the energy minimizing the voltage change across capacitors needed for various operation during the data conversion.

Technology: 65nm CMOS

Xiang Gao:

Low Jitter Low Power Phase Locked Loops Using Sub-Sampling Phase Detection @2010

Design of a clock generation Phase-Locked-Loop (PLL) with low jitter and low power. Using subsampling to reduce divider noise resulting in a Sub-Sampling-Phase-Locked-Loop (SSPLL).

Technology: 0.18µm CMOS

5: Circuit/System Receiver Solutions:

Bart Thijssen:

IoT receiver Techniques @2019

System and CMOS architectures improving IoT receivers and reducing power consumptions.

Technology: 22nm FD-SOI.

Anoop Bhat:

Wide Band Linearization Techniques for RF Receiver Front-Ends @2022

A wideband IF linear down-conversion-based receiver is presented together with a wideband linear active balun driving gigahertz ADC's

Technology: 22nm FDSOI

Claudia Palattella:

DTC for spur correction in Digital Frequency Synthesis @2019

Spur reduction technique based on DTC correction for flexible digitally programmable frequency synthesis.

Technology: 65nm CMOS

TRANSMITTERS:

6: RF

Saqib Subhan:

Cognitive Radio Transmitter with Broadband Clean Frequency Spectrum @2014

Realizing an 8-path Cognitive Radio Transmitter with clean frequency spectrum from 100MHz to 800MHz >= 40dB

Technology: 60nm CMOS

7: Amplifiers

RF:

Ali Ghahremani:

Switched-Mode Class E Power Amplifiers @2020

Designing high-performance and reliable switched-mode Class E power amplifier
Technology: 65nm CMOS

Anton Atanasov:

A Self-Matching Balanced Load Pull RF Antenna Amplifier @2024

The Self-Matching Balanced Amplifier (SMBA) is a power-efficient and mismatch-tolerant power amplifier (PA) architecture consisting of two active devices, which achieve impedance matching by actively load-pulling each other. This is done by means of a specially designed output matching network, allowing the active devices to see very low load impedances. The transistors (Ampleon BLP9G0722-20) are differentially excited, and together with the active matching, are less susceptible to power loss due to reflections from output load mismatch effects than a conventional balanced PA. This makes the SMBA very suitable for applications where it is important to deliver as much power as possible under strong load mismatch conditions, such as industrial heating, magnetic resonance imaging, and active phased arrays amongst others. The design has 40 MHz BW at 2.1 GHz and generates 48dBm output power with a gain of 16dB and drain efficiency of 43%.

LF:

Saifullah Amir:

Voltage Boosting Amplifier Techniques for Underwater Sensor Networks @2020

Design of a high-voltage amplifier for a piezoelectric transducer till 30kHz.

Technology: 0.25µm 60V TSMC

Audio

Chris Lokin:

Active PWM Ripple Reduction in Class-D Amplifiers using Digital Loop Filters @2022

A technique to reduce the ripple current after the output filter.
No chip was made but applied on an existing Digital Audio converter AX5689

D/A conversion

Erik Olieman:

Time interleaved High Speed D/A converters @2015

Power efficient very high speed D/A convertion using interleave current steering DACs

Technology: 65nm CMOS and 28nm FDSOI

Optical Applications

Vishal Agarwal:

Optocoupling in CMOS @2019

Avalanche Mode Light Emitting Diodes (AMLEDs) as transmitters and Single Photonic Avalanche Diodes (SPADs) as receivers in CMOS.

Technology: 140nm SOI CMOS

Photodiodes in CMOS:

Sasa Radovanovic:

High Speed photodiodes in standard CMOS technology @2004

A project of Fiber-to-the-Chip with the emphasis on the receiver side.

Technology: 1µm CMOS

Datatransmission:

On-Chip

Eisse Mensink:

High Speed Global On-Chip Interconnects and Transceivers @2007

Decreasing scaling in CMOS changed the speed of interconnects on-chip. Research on modelling and design of interconnects on chip.

Technology: 0.13µm CMOS

Daniël Schinkel:

On-Chip data communication @2011

Analysis, optimization, Circuit designs on transceivers shows clear improvement in speed on chip.

Technology: 130µm and 90nm CMOS

On PCB and cables:

Jan Rutger Schrader:

Wireline Equalization using Pulse-Width Modulation @2007

Equalization and modulation techniques

Technology: 130µm and 90nm CMOS

Photo’s Federico:

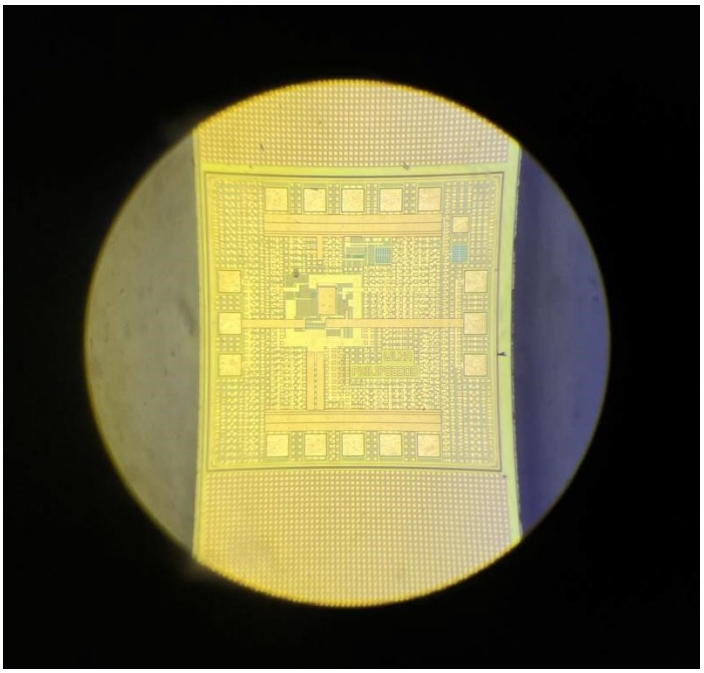
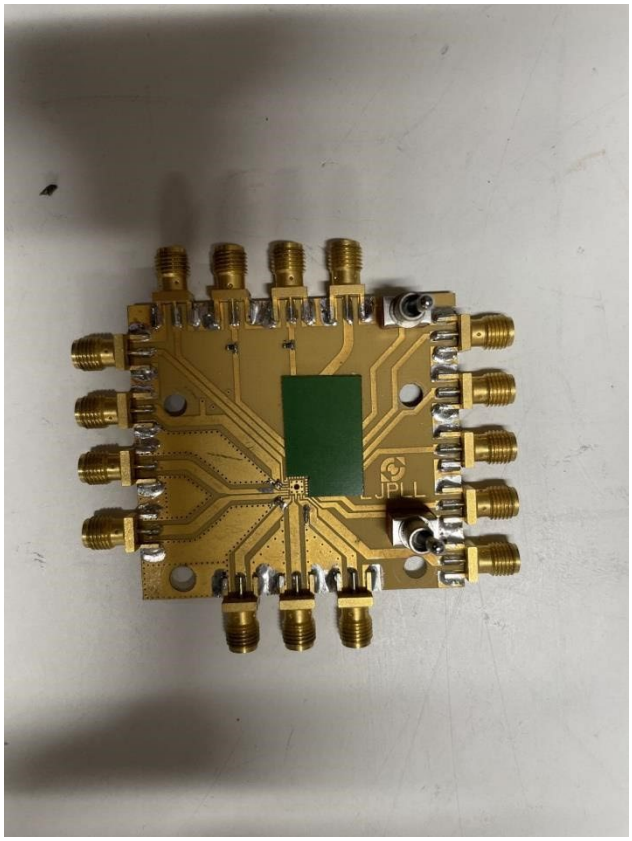
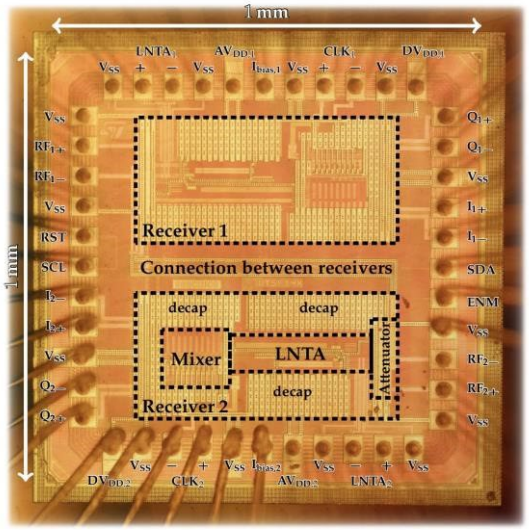


Photo X Gao

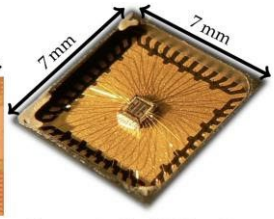


Photo’s Mark Oude Alink:



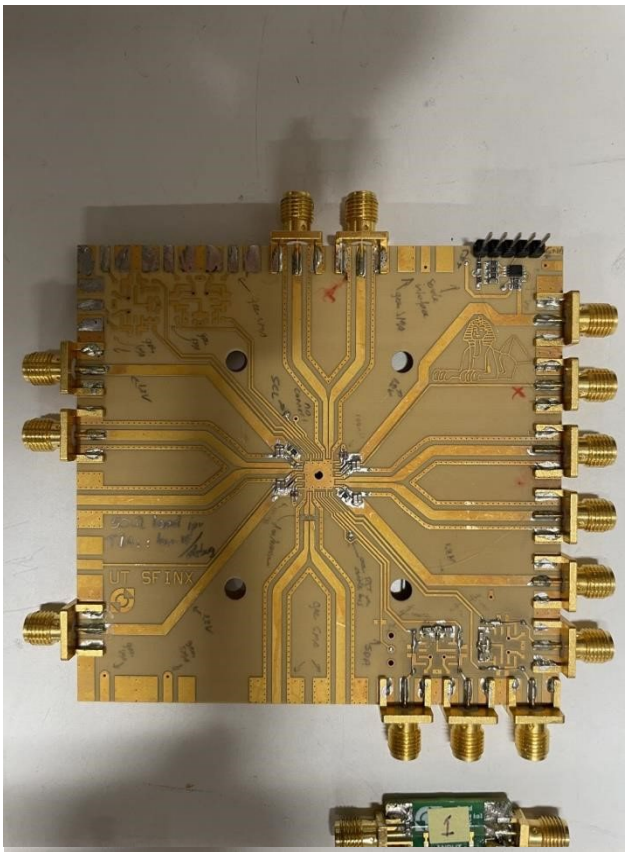
(a) Chip micrograph of UTSFINX,

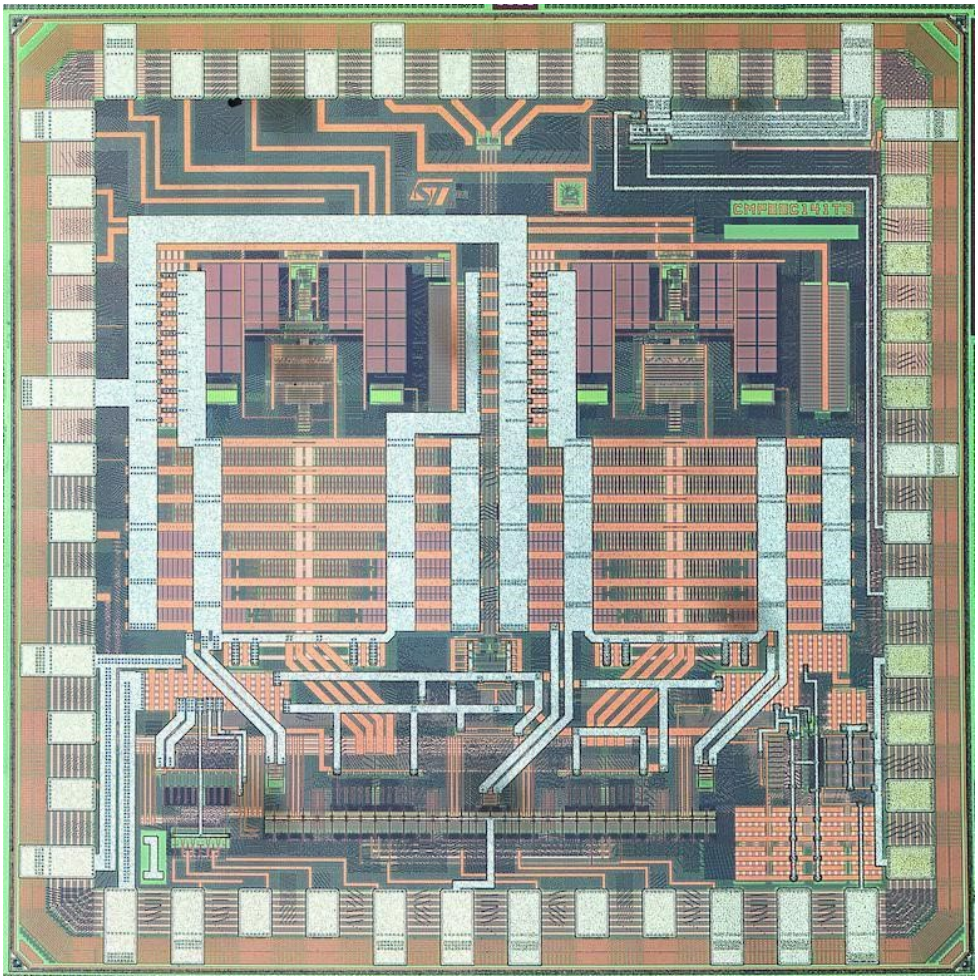
(b) Zoom-in on logo



(c) UTSFINX inside a QFN44-package

UTSFINX is fabricated in the 65 nm bulk CMOS process of ST.





Technology: 22 nm FD-SOI

Arnoud van de Wel:

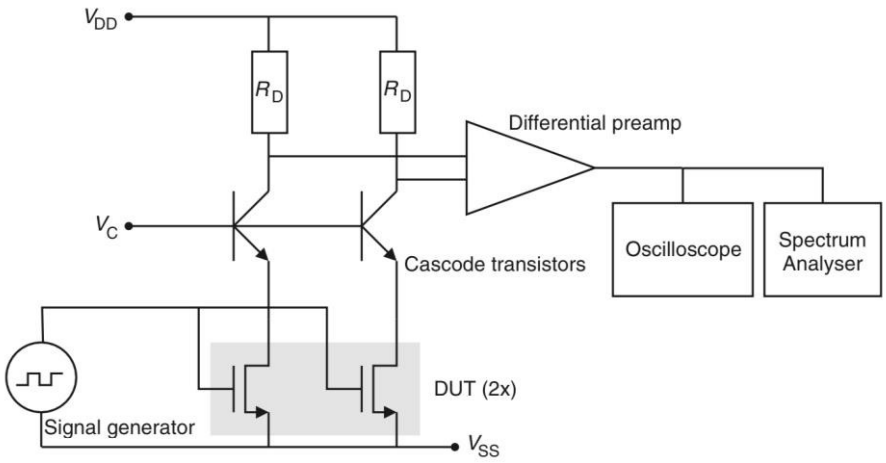
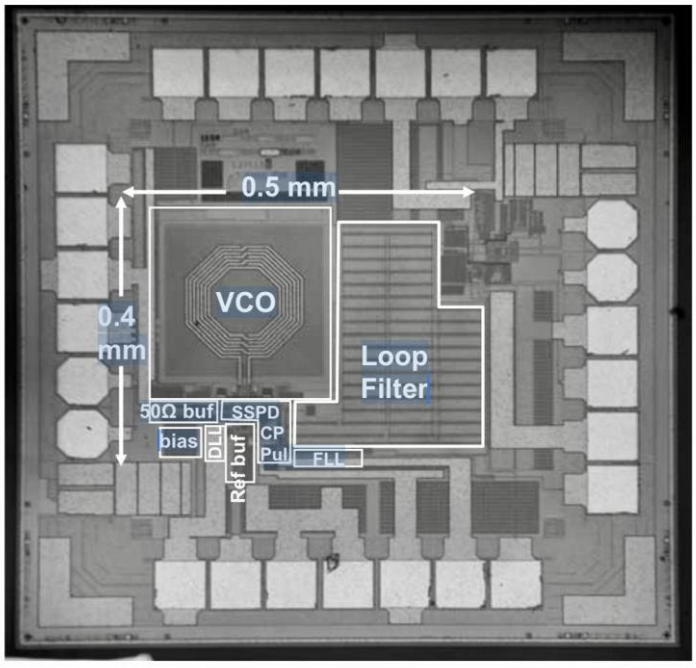
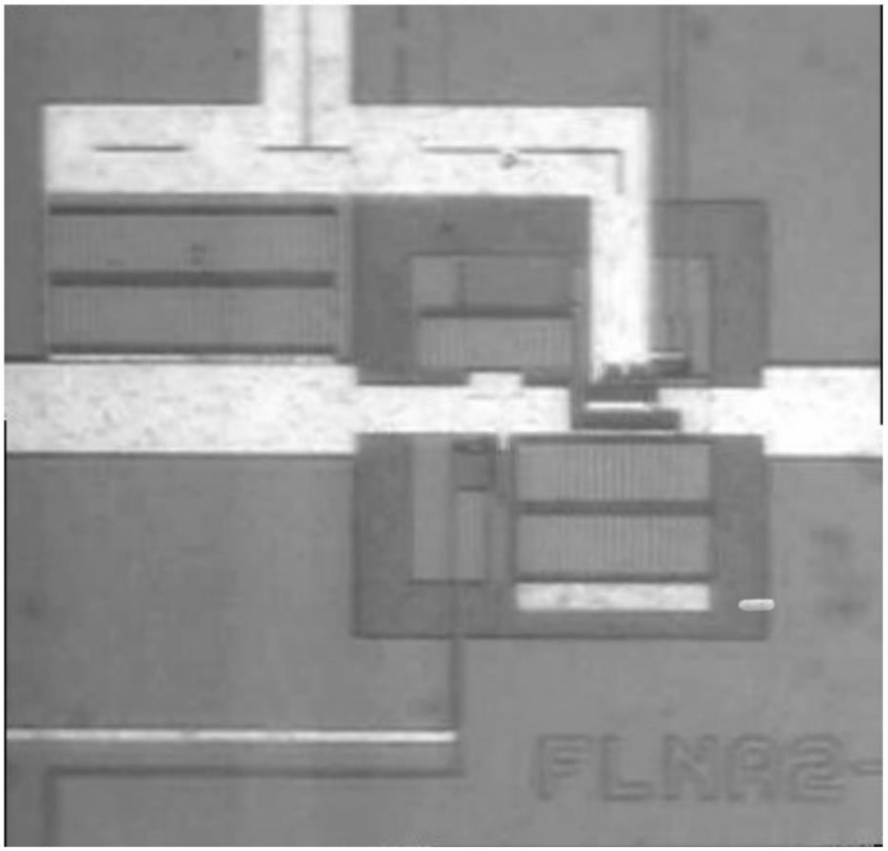
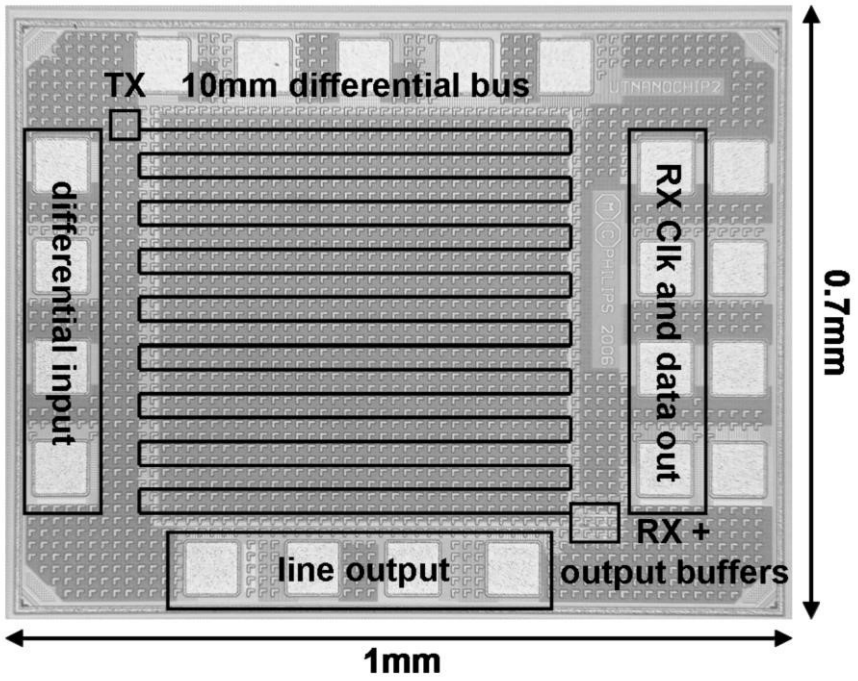
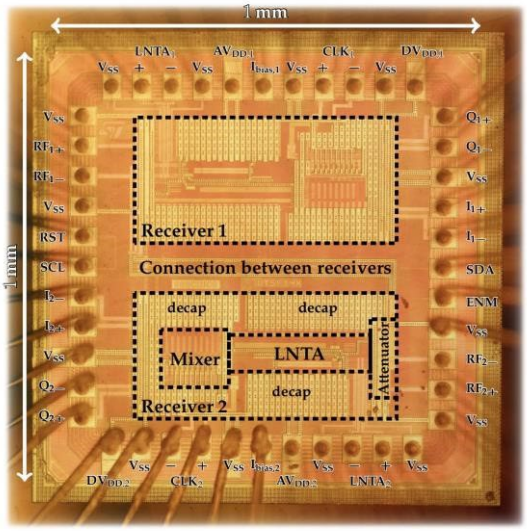


Figure 3.8: Noise measurement setup to measure LF noise in steady state and under LSE

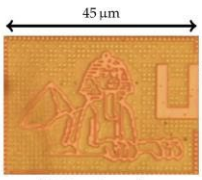




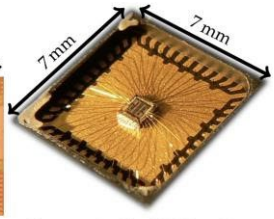

TX
10mm differential bus
differential input
RX Clk and data out
RX +
output buffers
line output
0.7mm
1mm



(a) Chip micrograph of UTSFINX,

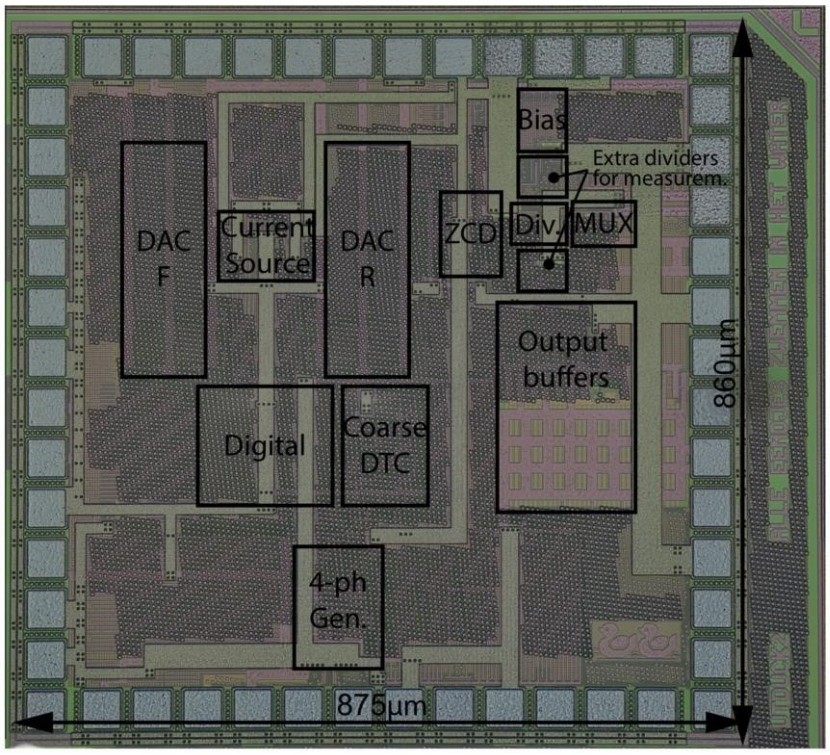


(b) Zoom-in on logo

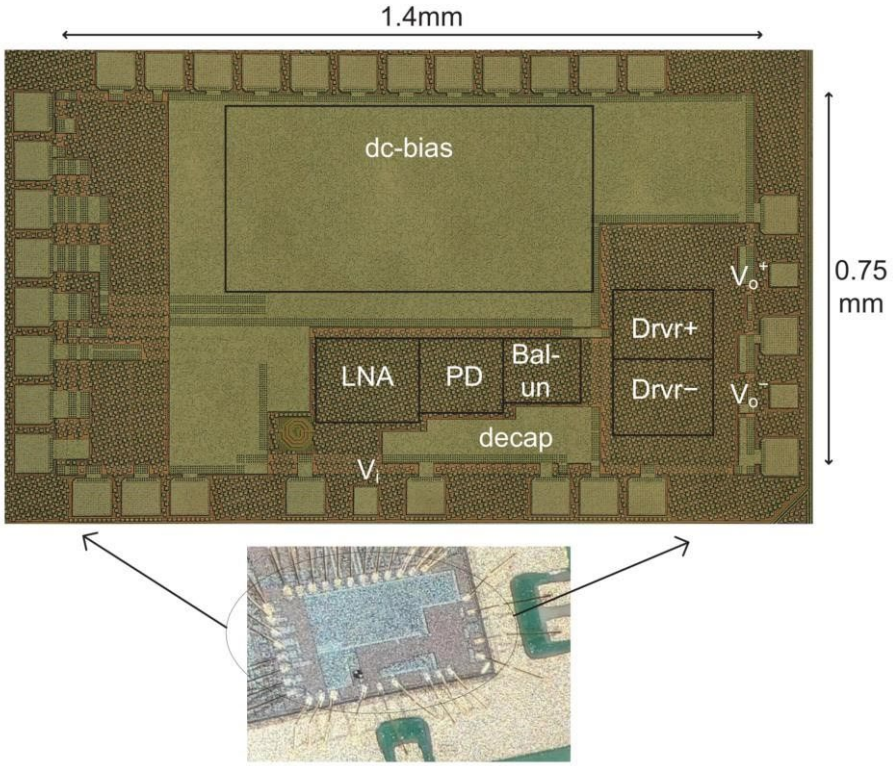


(c) UTSFINX inside a QFN44-package

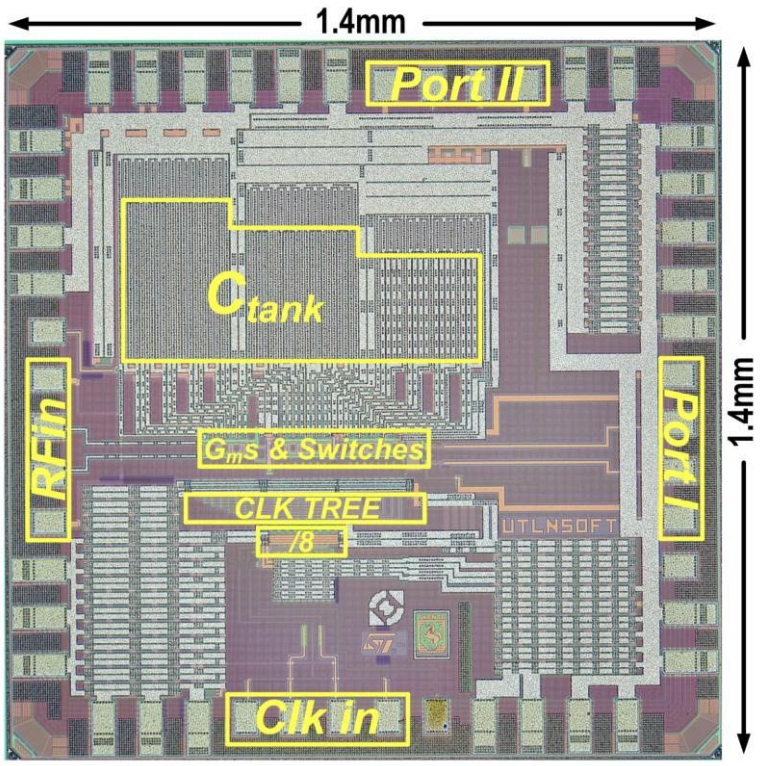
UTSFINX is fabricated in the 65 nm bulk CMOS process of ST.



Chip micrograph of UTDUCK



Chip photograph showing the placement of various blocks; the chip is directly mounted on a PCB and wire-bonded.



CMOS LP 65 nm chip micrograph

Noise Reduction

Analog

Digital

Physical way

On-Chip

On-Chip

On-PCB

Copper wires

[i]